Problem 1. (24 points) A and B are 9-bit registers that contain the binary values: $A = 100011101$ and $B = 111110000$.

(a) (4 pts) A third 9-bit register R is used to store the result of the micro-operation $R \leftarrow A+B$. What will be the binary value in R as well as the two most significant output carries, c_8 and c_9, of the addition?

```
Carry:  11111100000
A:        100011101
B:      + 111110000
          ---------
R:        100001101
```

(b) (4 pts) If the numbers in A and B are considered unsigned numbers, does R contain the correct result of $A + B$? Justify your answer.

No, because there is "1" carry out of the 9th bit after the addition, and A, B are two unsigned numbers

(c) (4 pts) If the numbers in A, B and B are considered signed numbers, represented in their 2's complement format, then does R contain the correct result of $A + B$? Justify your answer.

Yes, because:
the carry out of 9th and 8th bits are the same;
or,
the sign bit of the operands are the same with the result's sign bit (A_8=B_8=R_8=1)

2.

(a) (6 pts) If now the micro-operation $R \leftarrow A - B$ is executed, what will be the result stored in R as well as the last two output carries, c_8 and c_9, of the subtraction?

A – B = A + (2's complement of B) = A + B' + 1

Carry:	**00**00111111**1**
A:	100011101
B':	+ 000001111
R:	100101101

(b) (6 pts) If the numbers in A and B are considered signed numbers, represented in their 2's complement format, does R contain the correct result of the subtraction? Justify your answer.

Yes, because the carry out of 9th and 8th bits are the same; or, a negative number plus a positive number won't cause the overflow

Problem 2. (42 points) In this problem, you will desgin a 3-bit ALU to perform the micro-operations described in Table 1. The ALU takes its operands from two 3-bit registers $A = A_2A_1A_0$ and $B = B_2B_1B_0$, and returns an output $F = F_2F_1F_0$. In the case of arithmetic operations, assume that the contents of A and B are signed numbers in 2's compelement representation.

Table 1: Function table of a 3-bit ALU.

Selection				
S_2	S_1	S_0	Operation	Description
0	0	0	$F = A - 1$	Decrement by 1 (Décrémentation par 1)
0	0	1	$F = A - B$	Subtruction (Soustraction)
0	1	0	$F = A - 2$	Decrement by 2 (Décrémentation par 2)
0	1	1	$F = A - B - 1$	Subtraction with borrow (Soustraction avec emprunt)
1	0	0	$F = \overline{A} \vee B$	Logic implication (Implication logique)
1	0	1	$F = A \oplus B$	Comparison (Comparaison)
1	1	0	$F = cir\ A$	Circular shift right (Décalage circulaire à droite)
1	1	1	$F = ashl\ A$	Arithmetic shift left (Décalage arithmétique à gauche)

1. Design of arithmetic unit

(a) (10 pts) Draw a detailed logic circuit of the ALU's arithmetic unit.

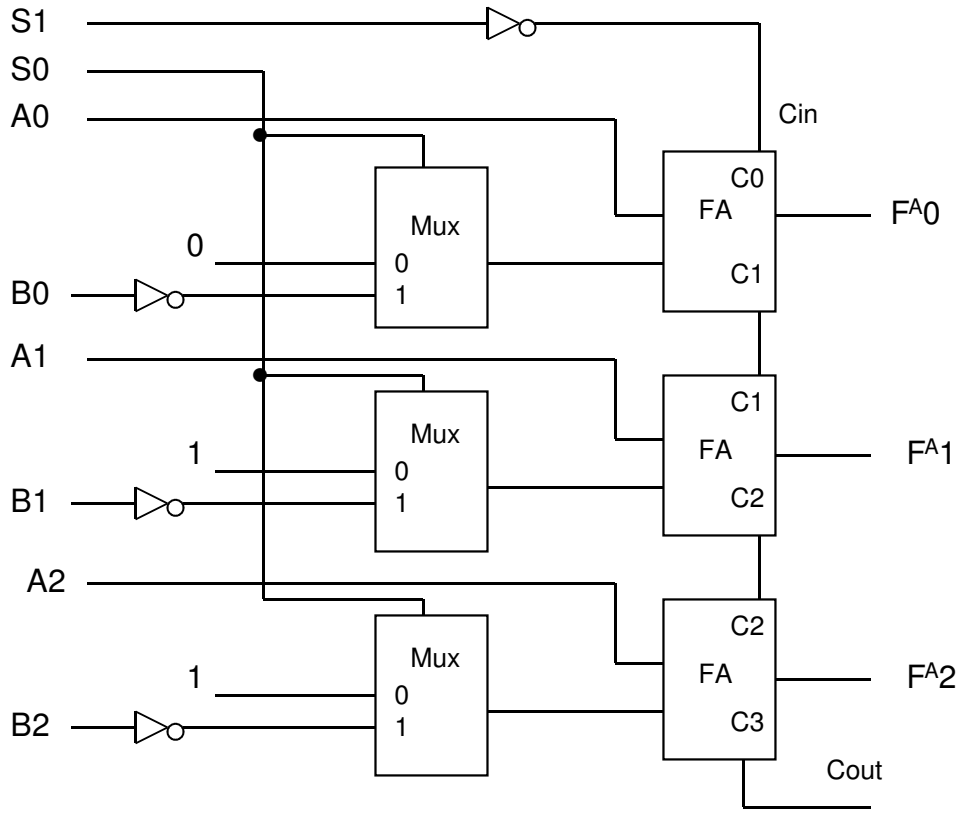
S_2	S_1	S_0	Operation	Description
0	0	0	$F = A - 1$	Decrement by 1 (Décrémentation par 1)
0	0	1	$F = A - B$	Subtruction (Soustraction)
0	1	0	$F = A - 2$	Decrement by 2 (Décrémentation par 2)
0	1	1	$F = A - B - 1$	Subtraction with borrow (Soustraction avec

F^0=A-1=A+2's(001) = A+111=(A+110)+1
F^1=A-B=A+2's(B2 B1 B0)=A+(B2' B1' B0'+1)

F^2=A-2=A+2's(010) = (A+110)
F^3=A-B=A+2's(B2 B1 B0)-1=A+(B2' B1' B0'+1)-1
=A+(B2' B1' B0')

$F^0=F^2+1 \Rightarrow F^{0,2}$ = (A+110)+S1'
$F^1=F^3+1 \Rightarrow F^{1,3}$ = (A+B2'B1'B0')+S1'

F^A = S0' $F^{0,2}$ + S0 $F^{1,3}$ =
= S0' [(A+110)+S1'] + S0 [(A+B2'B1'B0')+S1']



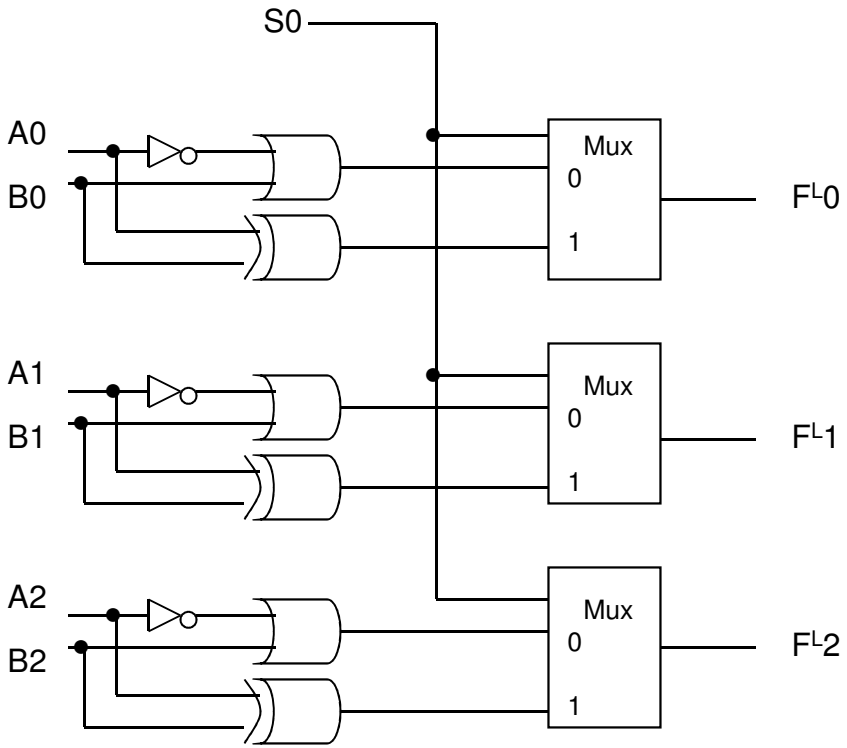
(b) (3 pts) A Boolean variable W is set to 1 when an overflow occurs and is reset to 0 otherwise. Find a simplified Boolean expression of W.

$W = C3 \oplus C2$

2. Design of logic unit

Draw a detailed logic circuit of the ALU's logic unit.

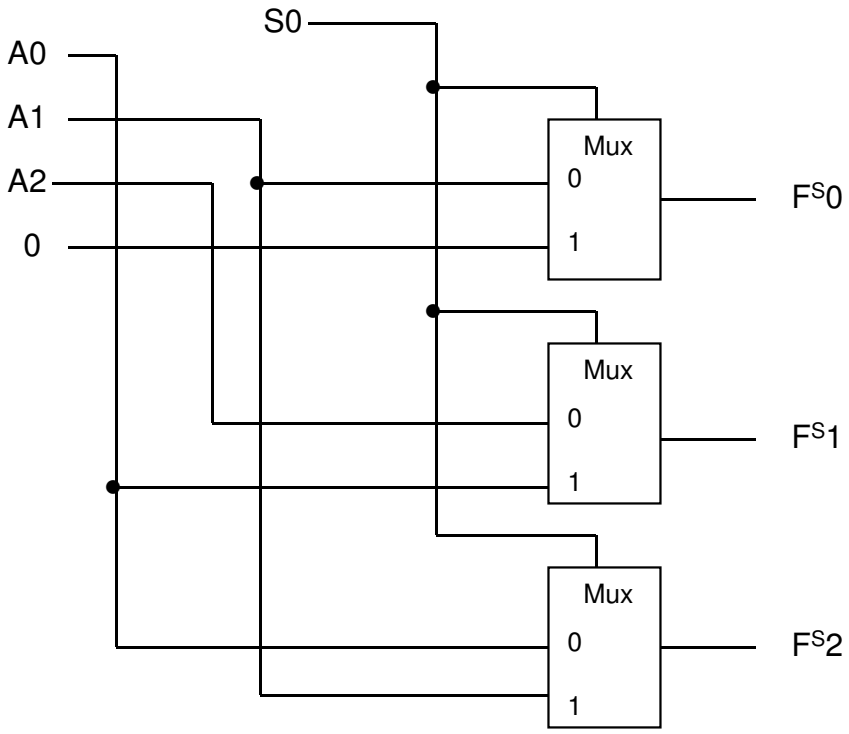
1	0	0	$F = \overline{A} \vee B$	Logic implication (Implication logique)
1	0	1	$F = A \oplus B$	Comparison (Comparaison)



3. Design of shift unit

(a) (8 pts) Draw a detailed logic circuit of the ALU's shift unit.

1	1	0	$F = cir\ A$	Circular shift right (Décalage circulaire à droite)
1	1	1	$F = ashl\ A$	Arithmetic shift left (Décalage arithmétique à gauche)



cir A : $A_2 A_1 A_0 \Rightarrow A_0 A_2 A_1$

ashl A : $A_2 A_1 A_0 \Rightarrow A_1 A_0 0$

(b) (3 pts) A Boolean variable V is set to 1 when an overflow occurs during the arithmetic shift and is reset to 0 otherwise. Find a simplified Boolean expression of V.

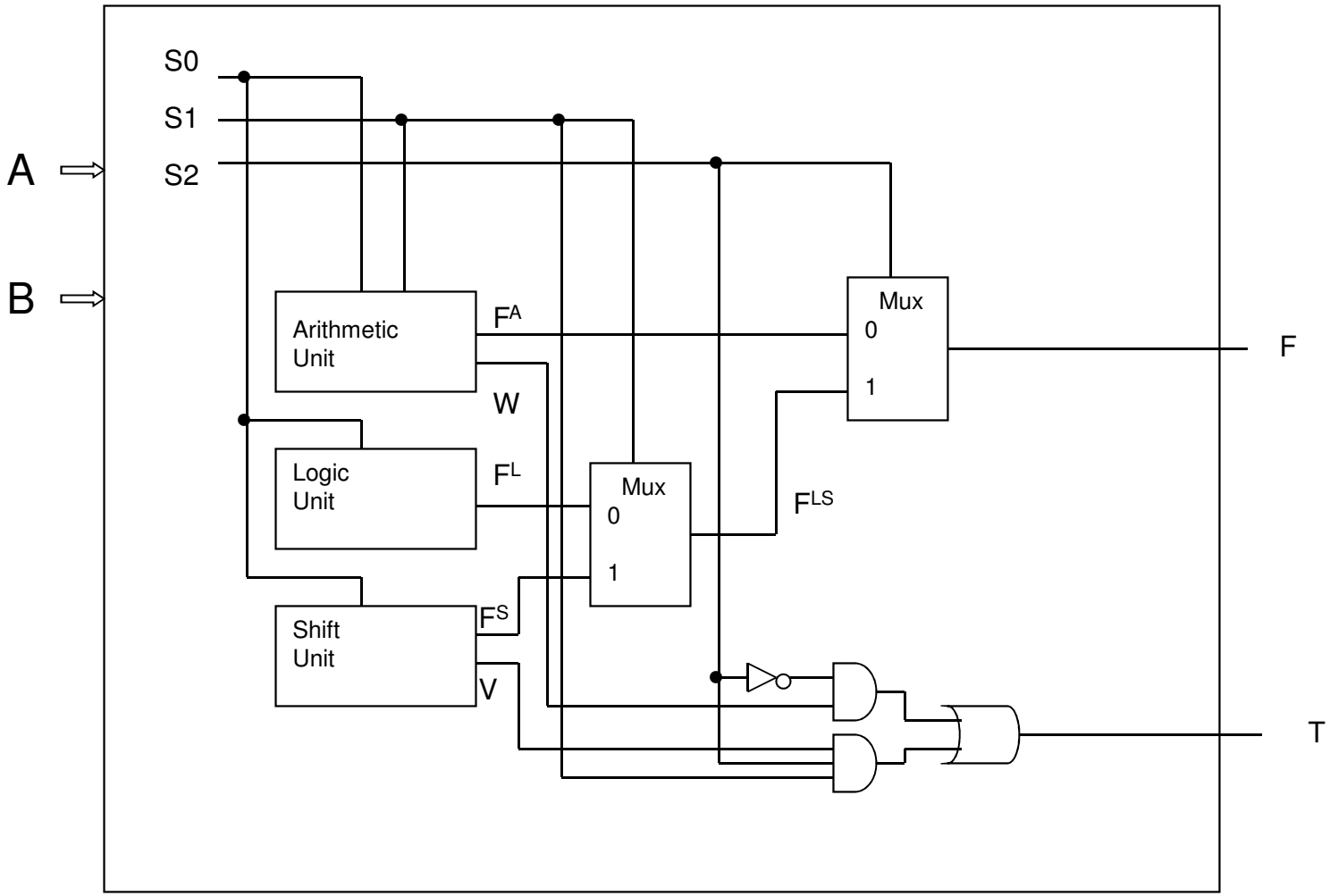
$$V = S0 (A2 \oplus A1)$$

4. Finalizing the ALU design

(a) (4 pts) A Boolean variable T is used to determine if one the micro-operations stated in Table 1 caused an overflow. T is set to 1 when an overflow occurs and is reset to 0 otherwise. Find a simplified Boolean expression of T. (*Hint:* express T in terms of W and V, and possibly other Boolean variables).

$$T = W S2' + V S2 S1$$

(b) (6 pts) Use bloc diagrams of the arithmetic, logic and shifting units in order to draw the bloc diagram of the complete ALU, including the overflow detection bit T.



Probleme 3. (34 points) Figure 1 shows the state diagram of a logic circuit which has a unique one-bit external input x.

1. Start by deriving the state table of the circuit. Then, assuming that JK flip-flops are to be used in the implementation, extend the state table with the excitation table of the circuit.

Present State$^{(n)}$		Input	Next State$^{(n+1)}$		Flip flop inputs			
Q_1	Q_0	X	Q_1	Q_0	J_1	K_1	J_0	K_0
0	0	0	0	0	0	x	0	x
0	0	1	0	1	0	x	1	x
0	1	0	0	0	0	x	x	1
0	1	1	1	1	1	x	x	0
1	0	0	x	x	x	x	x	x
1	0	1	x	x	x	x	x	x
1	1	0	0	1	x	1	x	0
1	1	1	1	1	x	0	x	0

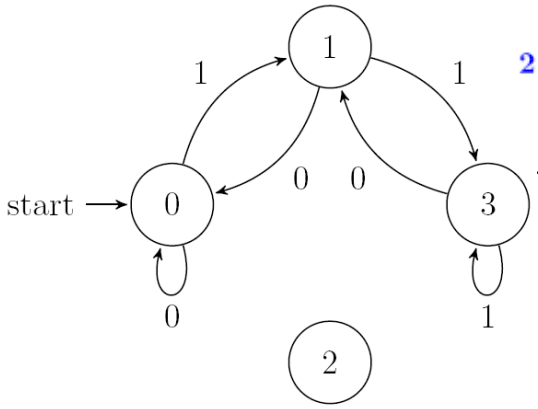


Figure 1: State diagram

2. Find simplified expressions for each flip-flop inputs.

Q_1 \ Q_0X	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$J_1 = Q_0 X$

Q_1 \ Q_0X	00	01	11	10
0	X	X	X	X
1	X	X	0	1

$K_1 = \overline{X}$

Q_1 \ Q_0X	00	01	11	10
0	0	1	X	X
1	X	X	X	X

$J_0 = X$

Q_1 \ Q_0X	00	01	11	10
0	X	X	0	1
1	X	X	0	0

$K_0 = \overline{Q_1}\,\overline{X}$

3. Draw the logic circuit using JK flip-flops and the minimum number of simple logic gates (AND/OR/NOT)